What Is Claimed:

1. A method for forming a bonded semiconductor-on-insulator substrate for semiconductor devices and integrated circuits, said method comprising:

providing a wafer comprising a monocrystalline semiconductor material;

implanting ions of the semiconductor material through a surface of the monocrystalline semiconductor wafer to a selected depth in said wafer, thereby forming adjacent to said surface an amorphous layer of the semiconductor material, said amorphous semiconductor layer extending to a substantially planar zone disposed at substantially said selected depth and comprising monocrystalline semiconductor material damaged by lattice defects, undamaged monocrystalline semiconductor material below said selected depth comprising a first layer of the monocrystalline semiconductor material;

heating said wafer under conditions effective to convert said amorphous semiconductor layer to a second layer of the monocrystalline semiconductor material;

heating the wafer under conditions effective to coalesce said zone of monocrystalline semiconductor material damaged by lattice defects, thereby forming a substantially planar intrinsic gettering zone comprising substantially pure semiconductor material and including active gettering sites, said gettering zone being disposed substantially at said selected depth;

providing a handle wafer comprising on one surface an insulating bond layer; and

bonding said insulating bond layer to said surface of said wafer, thereby forming a bonded semiconductor-on-insulator substrate comprising a handle wafer, an insulating bond layer, and a monocrystalline semiconductor device wafer, said device wafer containing a substantially planar intrinsic gettering zone that comprises substantially pure semiconductor material and includes active gettering sites.

2. The method of claim 1 wherein said monocrystalline semiconductor material comprises silicon and said implanted ions comprise silicon ions.

3. The method of claim 2 wherein said handle wafer comprises silicon and said insulating bond layer comprises silicon dioxide.

4. The method of claim 1 wherein the wafer of monocrystalline semiconductor further comprises a layer of oxide disposed on its surface, said ions of semiconductor material being implanted through said oxide layer and said surface into said wafer.

5. The method of claim 4 wherein said layer of oxide has a thickness of about 1 nm to about 50 nm.

6. The method of claim 1 wherein said ion implanting is carried out with a dose of about 10^{14} to 10^{18} ions/cm^2 at an energy of about 50 keV to 250 keV.

7. The method of claim 1 wherein said ion implanting in said monocrystalline semiconductor wafer is to a selected depth of about 0.1 μm to about 2.0 μm.

8. The method of claim 7 wherein said ion implanting in said monocrystalline semiconductor wafer is to a selected depth of about 0.2 μm to about 0.6 μm.

9. The method of claim 1 wherein said first layer of monocrystalline semiconductor material has a thickness of about 0.1 μm to about 0.8 μm.

10. The method of claim 9 wherein said first layer of monocrystalline semiconductor material has a thickness of about 0.2 μm to about 0.4 μm.

11. The method of claim 1 wherein said zone of monocrystalline semiconductor material damaged by lattice defects has a thickness of about 0.2 μm to about 0.4 μm.

12. The method of claim 1 wherein said heating said wafer under conditions effective to convert said amorphous semiconductor layer to said second layer of monocrystalline semiconductor material is carried out at a temperature of about 450°C to about 1200°C for about 15 minutes to about 8 hours.

13. The method of claim 12 wherein said heating is carried out at a temperature of about 550°C to about 620°C. for about 2 hours to about 6 hours.

14. The method of claim 1 wherein said heating said wafer under conditions effective to coalesce said zone of monocrystalline semiconductor material damaged by lattice defects into said substantially planar gettering zone is carried out at a temperature of about 800°C to about 1200°C for about 1 hour to about 6 hours.

15. The method of claim 14 wherein said heating is carried out at a temperature of about 1000°C to about 1150°C for about 2 hours to about 4 hours.

16. The method of claim 14 wherein said gettering zone has a thickness of about 0.05 μm to about 0.2 μm.

17. The method of claim 16 wherein said gettering zone has a thickness of about 0.1 μm.

18. The method of claim 1 further comprising:

thinning said second layer of monocrystalline semiconductor material to a thickness of about 0.2 μm to about 20 μm.

19. The method of claim 18 further comprising:

depositing a layer of epitaxial monocrystalline semiconductor material on said thinned second layer of monocrystalline semiconductor material.

20. The method of claim 1 further comprising:

forming a semiconductor device on said second layer of monocrystalline semiconductor material or on a layer of epitaxial monocrystalline semiconductor material deposited on said second layer.

21. The method of claim 20 wherein said semiconductor device is formed on said epitaxial layer.

22. The method of claim 21 wherein said semiconductor device is selected from the group consisting of a bipolar junction transistor, a field effect transistor, a capacitor, a resistor, a thyristor, and combinations thereof comprising integrated circuits.

23. The method of claim 3 further comprising:

forming a semiconductor device on said bonded substrate.

24. A semiconductor device formed by the method of claim 21.

25. The semiconductor device of claim 24 wherein said device is selected from the group consisting of a bipolar junction transistor, a field effect transistor, a capacitor, a resistor, a thyristor, and combinations thereof comprising integrated circuits.

26. A semiconductor device formed by the process of claim 23.

27. The semiconductor device of claim 26 wherein said device is selected from the group consisting of a bipolar junction transistor, a field effect transistor, a capacitor, a resistor, a thyristor, and combinations thereof comprising integrated circuits.

28. A bonded semiconductor-on-insulator substrate for semiconductor devices and integrated circuits, said substrate comprising:

a wafer comprising a monocrystalline semiconductor material and having a first surface and a second surface, said wafer comprising a first layer of the monocrystalline semiconductor material adjacent to said first surface and a second layer of the monocrystalline semiconductor material adjacent to said second surface, and interposed between said first and second layers of the monocrystalline semiconductor material, a substantially planar intrinsic gettering zone comprising substantially pure semiconductor material and including active gettering sites,

an insulating bond layer disposed on said second surface of said wafer; and

a handle wafer bonded to said insulating bond layer.

29. The substrate of claim 28 further comprising:

a layer of epitaxial monocrystalline semiconductor material deposited on said second layer of monocrystalline semiconductor material.

30. The substrate of claim 28 wherein said monocrystalline semiconductor material comprises silicon and said implanted ions comprise silicon ions.

31. The substrate of claim 28 wherein said handle wafer comprises silicon and said insulating bond layer comprises silicon dioxide.

32. The substrate of claim 28 wherein said first layer of monocrystalline semiconductor material has a thickness of about 0.1 μm to about 0.8 μm.

33. The substrate of claim 28 wherein said second layer of monocrystalline semiconductor material has a thickness of about 0.2 μm to about 20 μm.

34. The substrate of claim 28 wherein said gettering zone has a thickness of about 0.05 μm to about 0.2 μm.

35. The substrate of claim 28 further comprising two or more devices and one or more trenches surrounding at least one of said devices for laterally isolating the surrounded device from the other device(s).

36. A semiconductor device formed on the second layer of monocrystalline semiconductor material of the substrate of claim 28 or on a layer of epitaxial monocrystalline semiconductor material deposited on said second layer.

37. The semiconductor device of claim 36 wherein said device is selected from the group consisting of a bipolar junction transistor, a field effect transistor, a capacitor, a resistor, a thyristor, and combinations thereof comprising integrated circuits.

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